1. A method for determining a specification of a synchronous digital circuit comprising:

accepting a first specification of a first asynchronous digital system, including accepting a specification of a plurality of data elements whose values define the state of the system and a first plurality of state transition rules for the asynchronous digital system; and

determining a specification of a synchronous digital circuit from the specification of the asynchronous digital system, wherein during at least some clocking periods the synchronous digital circuit makes a state transition equivalent to state transitions specified by a plurality of the state transition rules specified for the asynchronous digital system.

2. The method of claim 1 wherein each state transition rule includes a specification of a precondition that must be satisfied by the state of the system to apply the state transition rule, and a specification of a resulting state that is reached as a result of applying the state transition rule.

3. The method of claim 2 wherein the state transition rules are defined as a term rewriting system.

4. The method of claim 3 wherein the specification of the synchronous digital system is in a register transfer language.

5. The method of claim 1 further comprising scheduling the state transition rules including identifying one or more sets of conflicting state transition rules for which state transitions specified by different rules in one of the conflicting sets may conflict in their access to data elements of the system.

6. The method of claim 5 wherein determining the specification of the synchronous system includes determining said specification such that during any clocking period, the synchronous digital circuit makes states transitions equivalent to at most one state transition rule from each conflicting set of state transition rules.

7. The method of claim 6 wherein determining the specification of the synchronous system includes determining a specification of arbitration logic associated with each conflicting set of state transition rules such that the arbitration logic generates trigger signals that allow at most one state transition rule from the conflicting set of states to be applied in a single clocking period.

8. The method of claim 7 wherein the arbitration logic includes a round-robin priority encoder for generating the trigger signals.

9. The method of claim 1 further wherein determining the specification of the synchronous system includes determining a specification of arbitration logic that generates trigger signals for sets of state transitions rules such that the rules in each of said are applicable in at least some order to the asynchronous digital system.

10. The method of claim 1 further comprising:

transforming the first specification of the first asynchronous digital system into a second specification of a second asynchronous digital system, wherein the second specification includes a second plurality of state transition rules, and the second asynchronous digital system includes pipeline;

wherein at least some of the first state transitions rules each correspond to a plurality of the second state transition rules such that each of these corresponding rules of the second plurality of state transition rules is associated with a different stage of the pipeline.

11. The method of claim 1 further comprising:

adding a plurality of composite rules to the first specification, wherein each composite rule is associate with a plurality of the first state transition rules, and each state transition specified by one of the composite state transition rules is equivalent to a sequence of state transitions each specified by the first plurality of state transition rules.

12. The method of claim 1 wherein accepting the specification of the data elements further includes accepting a specification of an abstract data type, and wherein determining a specification of a synchronous digital circuit includes determining an implementation of the abstract data type.

13. The method of claim 12 wherein the abstract data type is a first-in-first-out queue, and the implementation of the abstract data type is a register.

14. The method of claim 1 wherein the synchronous digital circuit implements a computer processor, and state transitions of the asynchronous digital system are associated with changes in values stored in storage elements of the computer processor.

15. The method of claim 1 wherein determining the specification of the synchronous circuit further includes determining a preliminary specification of a digital circuit, and optimizing the preliminary specification a correspondence between the preliminary specification and the specification of the asynchronous digital system.

16. A method for determining a specification an asynchronous digital system comprising:

accepting a first specification of a first asynchronous digital system, including accepting a specification of a plurality of data elements whose values define the state of the system and a first plurality of state transition rules for the asynchronous digital system;

transforming the first specification of the first asynchronous digital system into a second specification of a second asynchronous digital system, wherein the second specification includes a second plurality of state transition rules, and the second asynchronous digital system includes pipeline;

wherein at least some of the first state transitions rules each correspond to a plurality of the second state transition rules such that each of these corresponding rules of the second plurality of state transition rules is associated with a different stage of the pipeline.

17. The method of claim 1 further comprising:

adding a plurality of composite rules to the first specification, wherein each composite rule is associate with a plurality of the first state transition rules, and each state transition specified by one of the composite state transition rules is equivalent to a sequence of state transitions each specified by the first plurality of state transition rules.

18. A method for specifying a digital circuit implementing an instruction set architecture for a computer processor comprising:

accepting a first specification of a first asynchronous digital system which implements the instruction set architecture, including accepting a first plurality of state transition rules, each rule specifying a classes of state transitions of the asynchronous digital system and including a specification of a precondition that must be satisfied to apply the state transition rule, and a specification of a resulting state that is reached as a result of applying the state transition rule;

transforming the first specification into a second specification of a second asynchronous digital system, wherein the second specification includes a second plurality of state transition rules, and the second asynchronous digital system includes pipeline, wherein at least some of the first state transitions rules each correspond to a plurality of the second state transition rules such that each of these corresponding rules of the second plurality of state transition rules is associated with a different stage of the pipeline;

adding a plurality of composite rules to the second specification, wherein each composite rule is associate with a plurality of the second state transition rules, and each state transition specified by the composite state transition rule is equivalent to a sequence of two state transitions each specified by the second plurality of state transition;

determining a specification of a synchronous digital circuit from the specification of the asynchronous digital system and the identified sets of conflicting state transition rules, wherein during at least some clocking periods, the synchronous digital circuit makes a state transition equivalent to state transitions specified by a plurality of state transition rules.

19. Software stored on a computer-readable medium for causing a computer to perform the functions of:

accepting a first specification of a first asynchronous digital system, including accepting a specification of a plurality of data elements whose values define the state of the system and a first plurality of state transition rules, each state transition rule specifying a classes of state transitions of the asynchronous digital system;

scheduling the state transition rules including identifying sets of state transition rules that can be applied concurrently without conflict; and

determining a specification of a synchronous digital circuit from the specification of the asynchronous digital system, wherein during at least some clocking periods the synchronous digital circuit makes a state transition equivalent to state transitions specified by a plurality of the state transition rules specified for the asynchronous digital system.